ABSTRACT OF THE DISCLOSURE

A method for recognizing a pattern in a design of an integrated circuit (IC), comprising identifying a pattern correspondence element in a pattern instance. A pattern tree corresponding to the pattern instance is built. A list of candidate design correspondence elements in a design instance of the IC are built. Iteratively, for each design correspondence element in said list of candidate design correspondence elements each rank in a tree representation of said design instance built around said each design correspondence element is compared with corresponding rank in said pattern tree.